

# GAIN CONTROL METHODS AND SYSTEMS IN AN AMPLIFIER ASSEMBLY

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## CROSS-REFERENCE TO RELATED APPLICATIONS

- [0001] This application is a continuation of U.S. Patent Application No. 10/353,939, filed January 30, 2003, entitled "Gain Control Methods and Systems in an Amplifier Assembly," which claims priority to U.S. Provisional Application No. 60/430,061, filed December 2, 2002, entitled "Amplifier Assembly with AGC for a Tuner," which are all incorporated herein by reference in its entirety;
- [0002] This application is related to U.S. Non-Provisional Application No. 10/353,940, filed January 30, 2003, entitled "Amplifier Assembly Including Variable Gain Amplifier, Parallel Programmable Amplifiers, and AGC," which is incorporated herein by reference in its entirety.

## BACKGROUND OF THE INVENTION

### Field of the Invention

- [0003] The present invention relates generally to variable gain amplifier (VGA) assemblies and components thereof, gain control in such assemblies, and applications of the same.

### Related Art

- [0004] VGA assemblies are known in the art. What is needed is a more linear, lower noise, less costly amplifier assembly for providing variable amplifier gain in a variety of applications, such as those including multiple tuners for cable television and data signal applications.

## SUMMARY OF THE INVENTION

[0005] Embodiments of the present invention are directed to an amplifier assembly and components/modules used therein, gain control in the amplifier assembly, and associated methods. An embodiment of the present invention is directed to an Automatic Gain Control (AGC) system of the amplifier assembly, comprising: a Variable Gain Amplifier (VGA) configured to amplify an input signal according to a gain, to produce an amplified signal; a detector configured to detect a power indicative of a power of the amplified signal; a comparator module configured to compare the detected power to a high threshold, a low threshold and a target threshold between the high and low thresholds; and a controller module configured to change the gain of the VGA so as to drive the detected power in a direction toward the middle threshold when the comparator module indicates the detected power is not between the high and low thresholds.

[0006] Other embodiments of the present invention are apparent from the ensuing description.

## BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0007] In the drawings, like reference numbers indicate identical or functionally similar elements.

[0008] **FIG. 1** is a block diagram of an example VGA assembly for use in a tuner.

[0009] **FIG. 2** is a block diagram of an example arrangement of the VGA assembly of **FIG. 1**.

[0010] **FIG. 3** is a block diagram of an example arrangement of a VGA, including an array of parallel gain stages, for use in the VGA assembly of **FIG. 2**.

[0011] **FIG. 4** is a block diagram of an example arrangement of an attenuated gain stage of the VGA of **FIG. 3**.

[0012] **FIG. 4A** is a block diagram of another example arrangement of a portion of an attenuated gain stage of the VGA of **FIG. 2**.

- [0013] FIG. 4B is a block diagram of an arrangement of multiple attenuated gain stages, which is based on the gain stage arrangement of FIG. 4A.
- [0014] FIG. 4C is a block diagram of another example arrangement of the VGA of FIG. 2, using the attenuated gain stage arrangements of FIGs. 4A and 4B, and including differential components.
- [0015] FIG. 5 is a block diagram of still another example arrangement of the VGA of FIG. 2, including single-ended components.
- [0016] FIG. 6 is a block diagram of another example arrangement of an attenuated gain stage.
- [0017] FIG. 7 is a circuit diagram of an example differential amplifier used in a differential gain stage of the VGA of FIG. 2.
- [0018] FIG. 8 is a gain response curve or transfer function for a gain stage of the VGA of FIG. 2.
- [0019] FIG. 9 is an illustration of an exemplary smooth and continuous ramp-shaped gain change (increase) over time for a gain stage of the VGA of FIG. 2.
- [0020] FIG. 10 is an illustration of an exemplary smooth and continuous ramp-shaped gain change (decrease) over time for a gain stage of the VGA of FIG. 2.
- [0021] FIG. 10A is an illustrative example of how the aggregate gain of the VGA of FIG. 2 may be changed in steps in the present invention.
- [0022] FIG. 10B is an example plot of an AGC power control signal versus time for the amplifier assembly of FIG. 2, corresponding to an example receive signal scenario.
- [0023] FIG. 11 is a block diagram expanding on a controller module and a tri-level AGC window comparator of the amplifier assembly of FIG. 2, according to an embodiment of the present invention.
- [0024] FIG. 12 is a block diagram of an example switch within a decoder and switch matrix of the amplifier assembly of FIG. 2.
- [0025] FIG. 13 is a block diagram of an example arrangement of a power detector of the amplifier assembly of FIG. 2.

- [0026] **FIG. 14** is a circuit diagram of an example arrangement of the tri-level AGC window comparator of the amplifier assembly of **FIG. 2**.
- [0027] **FIG. 15** is a circuit diagram of an example arrangement of a ramp generator portion of a signal generator of the amplifier assembly of **FIG. 2**.
- [0028] **FIG. 16** is a circuit diagram of an example arrangement of a reference signal generator portion, and an associated ramp window comparator, of the signal generator of the amplifier assembly of **FIG. 2**.
- [0029] **FIG. 16A** is a circuit/block diagram of an example process monitor of the amplifier assembly of **FIG. 1**.
- [0030] **FIG. 16B** is a circuit diagram of an example sense circuit module of the processor monitor of **FIG. 16B**.
- [0031] **FIG. 17** is a flowchart of an example method of controlling gain that may be performed in the amplifier assembly of **FIG. 2**.
- [0032] **FIG. 18** is a flow chart expanding on an initial gain setting step of the method of **FIG. 17**, according to an embodiment of the present invention.
- [0033] **FIG. 19** is a flow chart expanding on a gain change step of the method of **FIG. 17**, according to an embodiment of the present invention.
- [0034] **FIG. 20** is a flow chart of a low-level example method expanding on the gain change step of the method of **FIG. 17**, which focuses on operations performed by elements of a controller module of the amplifier assembly of **FIG. 2** during the gain change.
- [0035] **FIG. 21** is a flow chart of another example method of controlling VGA gain performed in the amplifier assembly of **FIG. 2**.
- [0036] **FIG. 22** is an example system in which the amplifier assembly of **FIG. 1** may be used.

## DETAILED DESCRIPTION OF THE INVENTION

### Glossary

AGC – automatic gain control.

CATV – Community Antenna Television.

CI – Control Interface.

CMOS – Complementary Metal Oxide Semiconductor.

FET – Field Effect Transistor.

IC – Integrated Circuit.

VGA – Variable Gain Amplifier.

QAM: Quadrature Amplitude Modulated.

QPSK: Quadrature Phase Shift Keyed.

Television (TV) Standards:

NTSC – National Television System Committee.

PAL – Phase Alternating Line.

SECAM – Sequential Color with Memory (French).

## I. Overview

**[0037]** In a Community Antenna Television (CATV) system (also referred to as cable TV), a plurality of signals are frequency division multiplexed onto one or more coaxial cables. The CATV system has a downstream band or aggregate signal (headend-to-user) and an upstream band or aggregate signal (user-to-headend). In the downstream band, there can be approximately 135 channels having frequencies that range from 50 MHz to 860 MHz. The individual downstream channels represent different television signals that can be a mixture of analog television signals or digital signals. The analog television signals are preferably NTSC or PAL compliant television signals. The digital television signals carry digital video or cable modem data (e.g. internet traffic), and are typically modulated using 64 QAM or 256 QAM. Other outputs include a buffered version of an input (bypass function) and out-of-band (OOB) control signals.

**[0038]** While the amplitude of each signal varies as a function of the information being transmitted on that channel, the amplitude of the combined signal on the cable will vary not only as a function of the amplitude of each of the individual signals, but also as a function of the phase and amplitude relationship of each channel with respect to the others. Thus, the overall amplitude of the signal will be time varying as the phase and amplitude of

each of the individual signals line up. As an example, an amplifier used in a tuner that receives the downstream signal has to have good distortion performance when 135 channels, each at 0 Decibel-milliVolts (dBmV), are fed to the amplifier input. When the input level is increased to +15 dBmV on each channel, the amplifier must attenuate the input level back down to the same output level as in the case when all channels were at 0 dBmV, while maintaining good distortion performance.

[0039] **FIG. 1** is a block diagram of an exemplary amplifier assembly 102 for use in a tuner for CATV, for example. Amplifier assembly 102 includes a VGA amplifier module 104, AGC control circuitry or module 106 for controlling a gain of the VGA amplifier module, a process monitor 108. Amplifier assembly 102 also includes a control interface (CI) 109 for controlling and monitoring amplifier module 104, AGC module 106, and process monitor 108, over a control bus 110. An external controller 112 controls and receives status information from amplifier assembly 102, over an external control bus 114 coupled to CI 109. External control bus 114 may be a digital control bus including serial data lines and a clock line, for example. CI 109 may be an analog or digital controller, and control bus 110 may be an analog or digital control bus.

[0040] Amplifier module 104 receives a signal 114 including downstream channels spanning 54-860 MHz, for example. Signal 114 may include TV channels formatted according to NTSC, PAL, or SECAM standards, for example. Signal 114 may also include channels carrying digital data. Amplifier module 104 amplifies receive signal 114 in accordance with a gain of the amplifier module and divides or power-splits the resulting amplified receive signal, to produce a plurality of individual, separate amplified receive signals 118(1)-118(n). Amplifier assembly 102 produces signals 118(1)-118(n) in parallel with one another. Each signal 118(i) represents an amplified version of receive signal 114. Each of amplified signals 118 is associated with its own gain, and thus, may have a different power level than the other of amplified signals 118. The interchangeable terms “gain” and “gain value” as used herein are general, and are intended to include positive,

negative or zero gain. Thus, an amplifier having a gain may amplify a signal at a first power level, to produce an amplified signal at a second power level. The second power level may be greater than, less than, or equal to the first power level, depending on whether the gain is positive, negative, or zero, respectively.

[0041] In response to a power level of one of amplified signals 118 (e.g., signal 118(2)), AGC module 106 generates one or more gain control signals 120 that collectively control the gain of amplifier module 104, and thus the power levels of output signals 118. As a power level of receive signal 114 varies, AGC module 106 adjusts the gain of amplifier module 104 so as to maintain the individual power levels of amplified signals 118 at substantially constant respective power levels.

[0042] FIG. 2 is a block diagram of an example arrangement of amplifier assembly 102, expanding on FIG. 1. Amplifier assembly 102 includes various circuit elements constructed on an integrated circuit (IC) substrate or chip 202, depicted in dashed-line. Such on-chip circuit elements are depicted within the dashed-line 202. Amplifier assembly 102 also includes various circuit elements external to IC substrate 202, depicted outside of the dashed-line 202.

[0043] Amplifier module 104 includes a first stage amplifier 204 followed by a plurality of, for example, five, parallel second stage amplifiers 206 for generating corresponding, separate parallel amplified signals 118. In an exemplary arrangement, first stage amplifier 204 is a VGA including an array of variable gain stages arranged in parallel with each other, each having an individual gain controlled responsive to a corresponding one of gain control signals 120.

[0044] In the arrangement of FIG. 2, VGA 204 is a differential amplifier, including differential inputs and differential outputs. A pair of differential signal lines 208 carry receive signal 114 to the differential inputs of VGA 204. Amplifier assembly 102 includes a resistor 204a coupled between input lines 208, external to IC chip 202. Together, resistor 204a and input attenuation of VGA 204 (not shown in FIG. 2, but discussed below), set an input impedance of amplifier assembly 102. VGA 204 includes one or more gain control inputs

**205** for receiving corresponding gain control signals **120**. In an arrangement, gain control signals **120** include bias or control currents. In an alternative arrangement, gain control signals include bias or control voltages.

[0045] VGA **204** amplifies receive signal **114** according to a gain of the VGA set by gain control signals **120**, and produces an intermediate amplified receive signal **210**. A pair of differential signal lines **212**, coupled between the differential output of VGA **204** and respective differential inputs of each of second stage amplifiers **206**, carry amplified signal **210** to the second stage amplifiers. Thus, each of parallel amplifiers **206** is fed with signal energy from a common input, e.g., the output of VGA **204**/lines **212**. Also, a termination circuit or output load **207** (described below in connection with FIG. 7) couples output lines **212** to a power supply rail of amplifier assembly **102**.

[0046] Each of second stage amplifiers **206** has a gain that is programmable through CI **109**. Thus, each of second stage amplifiers **206** is also a VGA. Programmable gain registers **214**, coupled to CI **109** and respective gain control inputs of second stage amplifiers **206**, hold respective gain values that program the gains of the corresponding amplifiers **206**. Each amplifier **206(i)** further amplifies amplified receive signal **210** in accordance with its respective gain set by the programmable gain in corresponding gain register **214(i)**, to produce respective amplified signal **118(i)**. As depicted in FIG. 2, each amplifier **118(i)** is a differential amplifier, and each amplified signal **118(i)** is a differential signal. Termination circuits or output loads **207'(1)-207'(n)** (where each of the loads **207'** is similar to load **207**) couple respective outputs of amplifiers **206(1)-206(n)** to a power supply rail of amplifier assembly **102**. The output of each second stage amplifiers **206(i)** is configured for driving its own load, for example, an individual tuner coupled to the output. Thus, amplifier assembly **102** is configured to drive multiple loads (such as tuners) in parallel.

[0047] In an arrangement, a first sub-plurality of second stage amplifiers **206** (for example, outside amplifiers **206(1)** and **206(n)**) have a common gain, that is, a programmed first gain, and a second sub-plurality of second stage



amplifiers **206** (for example, inner amplifiers **206(2)** through **206(n-1)**) have a common second gain, that is, a programmed second gain. In this arrangement, the second gain is less than the first gain. For example, a ratio of the programmed first gain to the program second gain may be in a range of ratios of between 1:1 to 2:1.

[0048] Amplifier assembly **102** also includes AGC control circuitry or module **106** coupled between the output of second stage amplifier **206(2)** and gain control inputs **205** of VGA **204**. In an alternative arrangement, ACG module **106** is coupled between the output of VGA **204** (e.g., to lines **212**) and gain control inputs **205**. AGC control circuitry **106** includes, in series, a power detector **216**, a comparator module **218**, and an AGC controller module **220**.

[0049] Power detector **216** detects a power level of output signal **206(2)**, and provides a detected power indicator **230**, that is, a power level signal **230**, to comparator module **218**. Power detector **216** detects the combined power of all of the frequency channels in output signal **206(2)** (which are the frequency channels in input signal **114**). Therefore, power level signal **230** is representative of this combined power. Comparator module **218** includes a tri-level AGC window comparator **222**, an upper threshold register **224**, a lower threshold register **226**, and a middle or target threshold register **228**. Threshold registers **224**, **226** and **228** provide respective upper (high), lower (low) and target power thresholds **224a**, **226a** and **228a** to respective comparison inputs of comparator **222**. Thresholds **224a-228a** may be programmed through CI **109**. Target threshold **228a** may be half-way between thresholds **224a** and **226a**, closer to threshold **226a**, or closer to threshold **224a**, as desired.

[0050] Comparator **222** receives power level signal **230** at a comparison input of the comparator. Comparator **222** compares power level signal **230** to thresholds **224a**, **226a** and **228a**, to produce a comparison result signal **232**. Comparison result signal **232** indicates where the detected power of signal **118(2)** (that is, power level signal **230**) is in relation to thresholds **224a-228a**. Together, upper threshold **224a** and lower threshold **226a** define an AGC window.

[0051] Controller module 220 includes a controller 233 that receives comparison result signal 232 and a clock 234 generated by a clock generator 236. Controller 233 generates a set of control signals 238 responsive to comparison result 232, and provides the control signals to a decoder and switch matrix 240 (also referred to as switch matrix 240). A signal generator 242, including an off-chip capacitor 244, generates a set of ramp and reference signals 246, and provides the ramp and reference signals to decoder and switch matrix 240. Decoder and switch matrix 240 generates gain control signals 120 in response to signals 246 and control signals 238.

[0052] CI 109 can assert control over, and collect status information from, controller module 220, through control interface registers 249. For example, CI 109 can command clock generator 236 to either start or stop generating clock 234. CI 109 can access status information in controller 233 indicative of a present gain setting of VGA 204. CI 109 can command controller 233 to set the gain of VGA 204 to any desired gain value. In normal AGC operation, controller module 220 adjusts the gain of VGA 204 responsive to comparison result 232. However, CI 109 can command controller 233 to hold the gain of VGA 204 fixed at a desired gain value, that is, controller 233 can be commanded to be non-responsive to comparison result signal 232. Essentially, this disables AGC operation in amplifier assembly 102. Since the gains of VGA 204 and second-stage parallel amplifiers 206 may be controlled through CI 109, an alternative arrangement of the amplifier assembly omits AGC module 106. In such an arrangement, the gain of the VGA module is controlled exclusively by CI 109.

[0053] In yet another mode of gain control operation, the output of power detector 216 can be turned off, and an external control voltage 250 can be substituted for the output of power detector 216. In other words, external control voltage 250 replaces signal 230.

[0054] In an arrangement, clock generator 236 is a relaxation oscillator based on alternately charging an on-chip capacitor (not shown in FIG. 2) with a reference current  $I_{ref}$  and discharging the capacitor with a current  $2I_{ref}$ . This action produces a 50% duty-cycle triangle wave on a terminal of the capacitor.

The control signals for the charge/discharge action are actually the clock output square wave.

[0055] The frequency of clock 234 can be tuned by changing the charge/discharge current to the capacitor. An example frequency tuning range is approximately 1.25 kHz to 80 kHz. An additional frequency tuning factor of 2x can be obtained by either reducing the on-chip capacitor in half, or making the capacitor 2x larger.

[0056] Oscillator 236 also includes a synchronous reset capability which does not produce glitches (i.e., undesired narrow pulse width outputs) on clock 234 when a RESET signal from CI 109 is asserted (e.g., set to a logic "1"). Likewise, when the RESET signal is set to logic "0," no glitch occurs. This is performed by logic circuitry within oscillator 236. This no-glitch action insures that the last-held-state of controller 233, when controller 233 is implemented as a state machine, is maintained at reset and seamlessly restarted when reset is finished. The purpose of this feature is to allow for clock-free operation of the state machine (e.g., controller 233), except when checking for gain corrections via an external controller (e.g., controller 112). This was done in case relaxation oscillator 236 produces spurious signals on its output 234.

[0057] Amplifier assembly 102 also includes process monitor 108. In response to commands issued over CI bus 110, process monitor 108 selectively couples various ones of its process monitor outputs to the CI bus 110.

[0058] Amplifier assembly 102 also includes a bandgap voltage reference circuit 260. The bandgap voltage reference circuit 260 produces multiple voltages, including a first fixed voltage that does not vary with temperature, power supply voltage VDD or process variations. An example fixed voltage is approximately 1.2 Volts (V). Circuit 260 also produces a second voltage that increases proportional to absolute temperature (PTAT), but does not change with VDD or process variations.

[0059] Circuit 260 may produce bias currents based on the fixed and PTAT voltages. For example, the fixed voltage is applied across various resistors

(both on- and off-chip **202**) to create correspondingly fixed bias currents used by various sub-circuits within the IC chip. In general, the bias currents on the order of 200  $\mu$ A are sent to each sub-circuit. Each sub-circuit then mirrors the currents, sometimes at fixed ratios (either up or down) to get the current(s) needed in each sub-circuit.

[0060] Likewise, the PTAT voltage is applied across various resistors (both on- and off-chip **202**) to create PTAT bias currents used by various sub-circuits within the chip. The PTAT currents would increase at temperature increases.

[0061] A substantial portion of the circuits of amplifier assembly **102** are constructed on IC chip **202**. However, input load resistor **204a**, capacitor **244**, and output load circuit **207** are external to IC chip **202**. A general advantage of using such external or off-chip components is that relatively cheaper off-chip components have relatively more accurate parameter values (e.g., resistance, capacitance, inductance, and so on) as compared to corresponding internal or on-chip components. For example, low-cost off-chip components typically have 5% tolerances for resistors and 10% tolerances for capacitors and inductors. Even tighter tolerances can be achieved for slightly more expensive off-chip components.

[0062] In alternative arrangements of the present invention, input resistor **204a** is on-chip. In yet another arrangement, output load circuit **207** is on-chip. Similarly, capacitor **244** may be provided on-chip. The parameter accuracy of the on-chip components in such arrangements may be achieved in a variety of ways. For example, switched resistor banks with calibration routines may be used to select a best-valued on-chip resistor among multiple resistors, and so on. In the case of an on-chip version of external capacitor **244**, which is a large capacitance capacitor, capacitor multipliers may be used.

[0063] In another alternative arrangement of amplifier assembly **102**, parallel second-stage amplifiers **206** are omitted whereby the output of VGA **204** drives subsequent processing stages.

## II. VGA

[0064] **FIG. 3** is a block diagram of an example arrangement **300** of VGA **204**. In the example arrangement depicted in **FIG. 3**, VGA **204** includes a plurality of individual gain stages **302** arranged in parallel with each other. Each gain stage **302(i)** receives a corresponding gain control signal **120(i)**. Each gain stage **302(i)** includes a variable gain amplifier **304(i)** having a gain controlled responsive to the corresponding gain control signal **120(i)**. In the example arrangement of **FIG. 3**, VGA **204** includes an array of seventy (70) variable gain stages **302**, however, any number of gain stages from 1-to-n may be used. If only one gain stage is used, then AGC module **106** generates only one corresponding gain control signal **120(i)**.

[0065] VGA **204** includes an input node **310** coupled to differential signal lines **208**. Gain stages **302** have their respective inputs **312** coupled to input node **310**. Similarly, their respective outputs **314** are coupled to an output summing node **316** that combines together the respective gain stage outputs. Summing node **316** may be a wire-OR, for example, or any other circuit that combines together the gain stage outputs. Summing node **316** may include multiple sub-combining nodes for combining subsets of the outputs of gain stages **302**. In an arrangement, input node **310**, each of the inputs **312** and outputs **314**, each gain stage **302 (i)**, and summing node **316** are differential. However, these elements are depicted as being single-ended in **FIG. 3**. In VGA **204**, gain stages **302** are considered to be arranged in parallel for at least the reason that their respective inputs are coupled to common input node **310**, and thus, all of the gain stages are fed, with signal energy, from the common input node. Furthermore, the respective outputs of the gain stages are combined together at summing node **316**.

[0066] In operation, each gain stage **302(i)** amplifies receive signal **114** in accordance with its individual gain ( $g(i)$ ) set by corresponding gain control signal **120(i)** to produce a corresponding amplified receive signal presented at its output **314(i)**. Summing node **316** combines together all of these individual amplified signals to produce composite or aggregate amplified signal **210**. Together, the array of parallel gain stages **302** establishes an aggregate gain of

VGA 204 that is equal to a sum of all of the individual gains of gain stages 302. The aggregate gain is controlled in accordance with gain control signals 120.

[0067] In the arrangement depicted in FIG. 3, VGA 204 includes a first subset 316 of non-attenuated gain stages, including gain stages 302(1)-302(20). First subset gain stages 316 have substantially equal respective maximum gains. Amplifier array 204 also includes a second subset 320 of attenuated gain stages, including gain stages 302(21)-302(70). In an example arrangement, second subset gain stages 320 have progressively decreasing maximum gains in the direction 302(21)-302(70). In another example arrangement, VGA 204 includes a third subset of constant-attenuated gain stages, e.g., gain stages 304(71)-304(90), added to the bottom of the structure depicted in FIG. 3. All of the third subset of gain stages have fixed, constant attenuation.

[0068] FIG. 4 is a block diagram of an example arrangement of an attenuated gain stage in the second subset or group of attenuated gains stages 320. Attenuated gain stage 302(i) includes an attenuator 402(i) followed by amplifier 304(i). Attenuator 402(i) may provide fixed or, alternatively, programmable attenuation.

[0069] FIG. 4A is a block diagram of another example arrangement of an attenuated gain stage. In the arrangement of FIG. 4A, a tap-point or junction 404(i) between attenuator 402'(i) and amplifier 304(i) of attenuated gain stage 302(i) is coupled to a next attenuated gain stage 302(i+1), and so on. The attenuator reference numeral 402' includes the prime suffix (') to indicate that the attenuator is shared between gain stages. The use of the attenuated gain stage of FIG. 4A in VGA 204 leads to a another parallel arrangement of attenuated gain stages, as depicted in FIG. 4B.

[0070] FIG. 4B is a block diagram of such a parallel arrangement 410 of attenuated gain stages. In arrangement 410, the attenuated gain stages are cascaded in parallel with each other such that the attenuated gain stages share attenuators. Arrangement 410 includes an attenuation ladder 412 coupled between input node 310 (not shown in FIG. 4B) and the inputs of the amplifiers of the attenuated gain stages. Attenuation ladder 412 includes a

string of series connected attenuators **402'**. Successive amplifiers **304(i)**, **304(i+1)**, and so on, have their respective inputs fed from corresponding successive taps **404(i)**, **404(i+1)**, and so on, of attenuation ladder **412**. That is, each attenuator **402'(i)** feeds both the input to amplifier **304(i)** and also the input to attenuator **402'(i+1)** of next gain stage **302(i+1)**, and so on. Thus, the successive taps are associated with increasing attenuation. In this arrangement, attenuated gain stage **302(i+1)** includes attenuator **402'(i)**, attenuator **402'(i+1)**, and amplifier **304(i+1)** connected in series with one another. Similarly, attenuated gain stage **302(i+2)** includes attenuator **402'(i)**, attenuator **402'(i+1)**, attenuator **402'(i+2)**, and amplifier **304(i+2)** connected in series with each other, and so on.

[0071] **FIG. 4C** is a block diagram of a differential arrangement **420** of VGA **204**, using the attenuation ladder configuration described above in connection with **FIG. 4B**. In arrangement **420**, input node **310**, amplifiers **304**, attenuators **402'**, and output combining node **316** are all differential. Attenuation ladder **412** includes cascaded attenuators **402'**. Each attenuator **402'(i)** includes resistors **422(i)**, **424(i)** and **426(i)** connected together as depicted in **FIG. 4C**. Together, external input resistor **204a** and internal attenuators, **402'** (for example, attenuation ladder **412**) set or control the input impedance of amplifier assembly **102**, that is, the impedance seen looking into the amplifier assembly along input lines **208**.

[0072] **FIG. 5** is a block diagram of a single-ended (that is, non-differential) arrangement **500** of VGA **204**. The amplifier arrangement of **FIG. 5** includes a resistor ladder **502**, including resistors **504**, coupled between input node **310**, specifically between node **506** and ground. Amplifiers **304(21)**-**304(70)** in the attenuated gain stages have their respective inputs tied to corresponding successive taps of resistor ladder **502**. In an alternative arrangement, the individual taps of resistor ladder **502** are coupled to outputs of amplifiers **320**, instead of to the inputs of the amplifiers.

[0073] **FIG. 6** is a block diagram of another example arrangement of attenuated gain stage **302(i)**. As depicted in **FIG. 6**, attenuated gain stage **302(i)** includes amplifier **304(i)** followed by attenuator **402(i)**.

[0074] In still another arrangement of VGA 204, attenuators are omitted, so that the parallel attenuated gain stages are simply amplifiers (e.g., FETs) sized smaller than the amplifiers of the parallel non-attenuated gain stages. Since the gain of an amplifier is proportional to its size, the smaller amplifiers provide less gain. The attenuated gain stage amplifiers have progressively decreasing sizes, and therefore, progressively decreasing maximum gains.

[0075] In each of the arrangements of VGA 204 depicted in FIGs. 3, 4B, 4C and 5, all of the gain stages are considered to be arranged in parallel with each other for at least the reason that they are fed from a common input node. Also, their individual outputs are combined together to produce an aggregate output, e.g., amplified signal 210.

[0076] In still another arrangement of the VGA, the attenuated gain stages may be omitted. In such an arrangement, all of the parallel gain stages have substantially the same maximum gain.

[0077] FIG. 7 is a circuit diagram of an example differential gain stage amplifier 304(i) used in the present invention, for example, in amplifier array 204. As depicted in FIG. 7, a pair of differentially configured amplifier transistors 708a and 708b have their respective gate terminals connected to complimentary differential nodes of input 312(i). The drains of transistors 708a and 708b are coupled to respective complimentary sides of output 314(i). Termination circuit 207 (also referred to as an output load circuit, and mentioned above in connection with FIG. 2) couples the drains of transistors 708a and 708b (and sources of corresponding differential transistors in all of the other amplifiers 304) to a power supply rail  $P_S$ , at power supply voltage VDD, for example. Specifically, in termination circuit 207, the drain of transistor 708a is connected to power supply rail  $P_S$  through series connected resistor 709a and inductor 710a, and a ferrite bead 711a connected in parallel with the series resistor and inductor. Ferrite bead 711a has the effect of a large value inductor in parallel with a large resistor. Also, the drain of transistor 708b is similarly coupled to rail  $P_S$  through resistor 709b, inductor 710b, and ferrite bead 711b.



[0078] The respective source-drain paths of transistors 708a and 708b are connected together and to a current mirror 712, at a common terminal 713. Current mirror 712 includes a diode configured transistor 714 coupled to a gain control input terminal 715 (part of gain inputs 205) of amplifier 304(i), and also to a gate of a transistor 716, which has its source-drain path connected between terminal 713 and ground. Thus, transistor 716 operates as the tail current transistor, and thus as a current source, for differential transistors 708. In operation, gain control signal 120(i), applied to current mirror 712, controls a current 720 flowing through the source-drain path of tail transistor 716. The differential gain ( $g(i)$ ) of amplifier 304(i) is controlled responsive to a magnitude of current 720. Thus, gain control signal 120(i) controls the gain ( $g(i)$ ) of amplifier 304(i) and corresponding gain stage 302(i). In a typical arrangement, transistor 714 is a fraction, for example, one-eighth, the size of transistor 716. Thus, tail current 720 is a multiple, for example, eight times as large as, of control current 120(i).

[0079] Referring again to FIG. 2, each second stage amplifier 206(i) may include a differential amplifier that is similar to the amplifier depicted in FIG. 7. As mentioned above, each second stage amplifier 206(i) has its differential output coupled to respective termination circuit 207'(i). Also, each termination circuit 207'(i) is substantially the same as termination circuit 207 depicted in FIG. 7. However, the component values used in each circuit 207'(i) may differ from the component values used in the other circuits 207', and from the component values used in circuit 207.

[0080] FIG. 8 is a gain response curve for gain stage 302(i) and gain stage 304(i). That is, FIG. 8 is a plot of gain stage gain ( $g(i)$ ) versus the amplitude of corresponding gain control signal 120(i). In the present invention, gain control signal 120(i) is a current signal  $I(i)$ . A given gain control signal 120(i) can set the gain of corresponding gain stage 302(i) to a minimum gain (e.g., zero gain), a maximum respective gain for that gain stage, or may cause the gain to change between its minimum value (e.g., zero) and the maximum value.

[0081] In the present invention, a gain change between the minimum and maximum gain levels for a given gain stage 302(i) is achieved according to (that is, follows) a ramp function. That is, the gain changes (e.g., increases or decreases) gradually over a time interval. In accordance with the ramp function, the gain changes smoothly and continuously to avoid abrupt, discontinuous gain changes.

### III. VGA Gain Change Operation - Overview

[0082] FIG. 9 is an illustration of such a smooth and continuous ramp-shaped gain change for a given gain stage 302(i). Specifically, FIG. 9 is an example combined plot for (i) gain versus time, and correspondingly, (ii) gain control current  $I(i)$  versus time, for gain stage 302(i). In the plot of FIG. 9, gain stage 302(i) undergoes a gain change (i.e., increase) from zero gain at time  $t_1$  to its respective maximum gain at time  $t_2$  in response to gain control current  $I(i)$ . The gain change is continuous, that is, does not have discrete gain level steps or jumps. Also, the gain change is smooth. For example, the slope of the gain change is continuous, and thus, does not exhibit discontinuities. The gain may increase monotonically over time, such as linearly or exponentially. However, the gain change may also include non-monotonic portions, as long as they are smooth and continuous.

[0083] FIG. 10 is combined plot similar to FIG. 9, but for a decrease in gain. That is, FIG. 10 is an illustration of an exemplary smooth and continuous ramp-shaped gain change (decrease) over time for a gain stage 302(i) of the VGA of FIG. 3.

[0084] FIG. 10A is an illustrative example of how the aggregate gain of first stage amplifier 204, e.g., amplifier array 204, may be changed in the present invention. In this illustrative example, the aggregate gain of amplifier array 204 is decreased from a maximum aggregate gain to an intermediate aggregate gain. In FIG. 10A, each gain stage 302(i) is depicted as a triangle. Dark-shaded triangles depict gain stages that are fully ON, that is, operated at their respective maximum gains. In contrast, triangles that are not shaded (that is,

un-shaded triangles) depict gain stages that are fully OFF, that is, gain stages set to zero gain. Triangles filled with cross-hatches indicate gain stages that are in the process of having their respective gains changed, for example, either increased or decreased. Also, the process of changing aggregate gain depicted in **FIG. 10A** proceeds from a first step “Step 1” depicted at the top of **FIG. 10A**, to a final step “Step 5” depicted at the bottom of the **FIG. 10A**.

[0085] Initially, in Step 1, the aggregate gain of amplifier array **204** is at a maximum aggregate gain level. In this state, all of non-attenuated gain stages **316** (i.e., gain stages **302(1)**-**302(20)**) are set to or operating at their respective maximum gains. Concurrently, all of the attenuated gain stages **320** (i.e., gain stages **302(21)**-**302(70)**) are set to or operated at zero gain. Thus, in Step 1, gain stages **302(1)** through **302(20)** represent first gain stages among the set of gain stages **302** that are set to their respective maximum gains. Similarly, gain stages **302(21)** through **302(70)** represent second gain stages of the gain stages **302** that are set to zero gain. Note here that the terms “first gain stages” and “second gain stages” refer to gain stages of **VGA 204** only, and are not to be confused with “first stage amplifier **204**” and “second stage amplifiers **206**” discussed above in connection with **FIG. 2**, for example.

[0086] In Step 2, the gain of one of the first gain stages is decreased to zero gain according to a ramp function and the gain of one of the second gain stages is increased to its respective maximum gain according to the ramp function. More specifically, the gain of gain stage **302(1)** is decreased to zero gain according to the ramp function and the gain of gain stage **302(21)** is increased to its respective maximum gain according to the ramp function. The gain increase operation and the gain decrease operation may be performed concurrently, or alternatively, sequentially, that is one after the other.

[0087] After the gain changes of Step 2, the amplifier array **204** is configured as depicted in Step 3 of **FIG. 10A**. Namely, gain stages **302(2)** through **302(21)** are set to the respective maximum gains (and thus, represent a new set of first gain stages that are fully ON), while gain stages **302(1)** and **302(22)**-**302(70)** are set to zero gain (and thus, represent a new set of second gain stages that are fully OFF).

[0088] In step 4, a further decrease in aggregate gain is achieved by decreasing the gain of gain stage 302(2) to zero and increasing the gain of gain stage 302(22) to its respective maximum. These gain changes may be performed concurrently or sequentially.

[0089] After the gain change of Step 4, amplifier array 204 is configured as depicted in Step 5. The aggregate gain of amplifier array 204 in Step 5 is less than the aggregate gain of amplifier array 204 in Step 1. This is because the sum of the maximum gains of the gain stages turned ON in Step 5 (i.e., gain stages 302(3)-302(22)) is less than the sum of the maximum gains of the gain stages turned ON in Step 1 (i.e., gain stages 302(1)-302(20)). State otherwise, the sum of the maximum gains of gain stages 302(20)-302(21) is less than the sum of the maximum gains of gain stages 302(1)-302(2).

[0090] During the gain change process depicted in FIG. 10A, a contiguous set of gain stages (e.g., twenty gain stages) are maintained in their fully ON states. This contiguous set of ON gain stages is dynamic, and “slides” to the right across the full set of gain stages 302 depicted in FIG. 10A. If the aggregate gain is further decreased to a point where the lower twenty attenuated gain stages, e.g., gain stages 302(51)-302(70)), are ON, then any further decrease in gain is achieved by sequentially turning OFF gain stage 302(51), then gain stage 302(52), and so on until none of the gain stages remain ON.

[0091] The process for increasing aggregate gain is essentially opposite from the process for decreasing aggregate gain. That is, higher numbered gain stages are sequentially turned fully ON, while lower numbered gain stages are sequentially turned fully OFF. In this case, the contiguous set of ON gain stages would slide to the left in FIG. 10A as the aggregate gain is increased.

[0092] FIG. 10B is an example plot of power control signal 230 versus time corresponding to an example receive signal scenario. The example plot of FIG. 10B serves as a useful illustration of the operation of VGA 204 and AGC module 106 with respect to power level signal 230 and thresholds 224a-228a. An initial assumption is that at a time  $t_0$ , the power of receive signal 114, the aggregate gain of VGA 204, and the resulting power of amplified receive signal 118(2) are such that power level signal 230 is between upper

threshold **224a** and lower threshold **226a**, as depicted in **FIG. 10B**. It is also assumed that at periodic time intervals  $t_{\text{sample}}$ , controller module **220** (more specifically, controller **233**) polls or “samples” comparison result signal **232**.

[0093] Beginning at a time  $t_0$ , a slow increase in the power of receive signal **114** causes a correspondingly slow increase in amplified signals **210** and **118(2)**, and power detector level signal **230**. AGC module **106** maintains the gain of amplifier **204** at a fixed level as power signal **230** rises. Eventually, power signal **230** rises to a level that is greater than upper threshold **224a**, as indicated at **1050** in **FIG. 10B**. At a next sample time **1052**, controller module **220** polls comparison result signal **232**, which indicates the over-threshold condition at **1050**. In response to this over-threshold condition, controller module **220** generates gain control signals **120** to decrease the gain of VGA **204** continuously and smoothly, and correspondingly, power level signal **230**, until the power level signal passes below target threshold **228a**.

[0094] At a sample time **1054**, controller module **220** becomes informed that power level signal **230** has crossed, e.g., dropped below, target threshold **228a**. In response to this condition, controller module **220** generates gain control signals **120** such that the gain of amplifier **204** remains fixed. That is, controller module **220** stops changing the gain amplifier **204** because power signal **230** is at or near the target threshold **228a**. Controller module **220** will cause the gain of amplifier **204** to remain at this fixed level until power level signal **230** again becomes either too high (i.e., above upper threshold **224a**) or too low (i.e., below lower threshold **226a**). Controller module **220** causes the gain of VGA **204** to decrease in a smooth and continuous manner between points **1050** and **1054**. This results in the smooth and continuous downward slope of power level signal **230** depicted in **FIG. 10B**. In an example arrangement, controller module **220** causes the gain of VGA **204** to decrease according to the process discussed above in connection with **FIG. 10A**, that is, by sequentially turning OFF and ON gain stages in the amplifier array **204**. The smooth and continuous gain change arrangement produces a correspondingly smooth and continuous change in the power levels of signals **210** and **118**.

[0095] The smooth and continuous change of power level signal **230** depicted in **FIG. 10B** includes small stair-steps or “wiggles” having sloped falling edges. This results from smooth and continuous gain changes having corresponding stair-steps. These stair-steps result from pauses between incremental gain changes. For example, with reference again to **FIG. 10A**, gain is changed in the following manner. In Step 2, the gain of VGA **204** is decreased an incremental amount, smoothly and continuously according to a ramp function. Then, in step 3, the gain of VGA **204** remains constant for a short period of time, that is, the gain remains level. Then, in Step 4, the gain of VGA **204** is decreased again an incremental amount, smoothly and continuously according to a ramp function. Steps 2, 3 and 4 repeat until power level signal **230** crosses target threshold **228a**. The pause between successive incremental gain changes is discussed below in connection with **FIG. 20**.

#### IV. Controller Module, Detector Module, and Comparator

[0096] **FIG. 11** is a block diagram expanding on controller module **220** and portions of comparator module **218**, discussed above in connection with **FIG. 2**. Depicted in **FIG. 11** are various low-level control signals not specifically depicted in **FIG. 2**. As mentioned above, controller module **220** generates gain control signals **120** responsive to comparison result signal **232**. Controller **233** of controller module **220** provides a comparator control signal **1102** to comparator **222**. At periodic time intervals, controller **233** asserts comparator control signal **1102**, thus causing comparator **222** to produce comparison result signal **232** at these time intervals. Thereafter, controller **233** polls comparison result signal **232** to determine whether the gain of VGA **204** should be either changed or maintained at a current or present level, as mentioned above in connection with **FIG. 10B**. In the present invention, the periodic time intervals (e.g., the time between successive polling operations) are programmable in duration, and should correspond to the rate at which the power level of input signal **114** is expected to vary. Exemplary time intervals may be between 1 millisecond and 1 minute, or even longer. More typical

time intervals are in the range of 1-10 milliseconds. In an arrangement, controller 233 is a state-machine based controller clocked by clock 234. However, controller 233 may be any digital or analog controller.

[0097] Controller 233 also provides signal generator control signals 1104 to signal generator 242, and receives a ramp status signal 1106 from the signal generator. Signal generator 242 includes a ramp generator and a reference signal generator (not shown separately in FIG. 11). The ramp generator generates complimentary ramp signals 1108 (VRAM\_P) and 1110 (VRAM\_N) on command, that is, in response to a ramp trigger signal in control signals 1104. The reference signal generator generates reference signals 1112 (VREF\_HI) and 1114 (VREF\_LO) having complimentary fixed signal values or amplitudes. For example, signal 1112 is a fixed high voltage, while signal 1114 is a fixed relatively low voltage. Signals 1108-1114 are provided to decoder and switch matrix 240.

[0098] Controller 233 also generates control signals 238 for controlling decoder and switch matrix 240. Control signals 238 include an address pointer 1116 indicating which of the gain stages 302 of VGA 204 should be fully ON, that is, operating at their respective maximum gains, at any given time. Controller 233 also generates a set of digital control signals 1120 for controlling various functions of decoder and switch matrix 240. For example, signals 1120 indicate whether the gain of VGA 204 should be increased or decreased, and when such a change should occur. Responsive to (i) control signals 1116 and 1120, (ii) ramp signals 1108 and 1110 when generated, and (iii) reference signals 1112 and 1114, decoder and switch matrix 240 generates gain control signals 120 as appropriate to either change (i.e. increase or decrease) or maintain at a constant level the gain of VGA 204.

[0099] FIG. 12 is a block diagram of a representative portion 1200(i) of decoder and switch matrix 240. Portion 1200(i) is repeated within decoder and switch matrix 240 for each of gain stages 302(i). Portion 1200(i) includes a switch 1204(i) that receives signals 1108-1114 and a control signal 1206(i) derived responsive to control signals 238 (that is, 1116 and 1120). In response to control signal 1206(i), switch 1204(i) connects either (i) ramp signals 1108

and 1110, or (ii) reference signals 1112 and 1114, to the inputs of a differential driver 1210(i). Differential drive 1210(i) generates gain control signal 120(i) responsive to its switched inputs.

[00100] More specifically, responsive to control signals 238, switch 1204(i) may be placed in any one of four different configurations. In a first configuration, switch 1204(i) connects reference signals 1112 and 1114 to differential driver 1210(i) such that gain control signal 120(i) has a static maximum amplitude that drives or sets the gain of corresponding gain stage 302(i) to a maximum value.

[00101] In a second configuration, switch 1204(i) connects reference signals 1112 and 1114 to differential driver 1210(i), in a manner that is inverted with respect to the first configuration, such that gain control signal 120(i) has a static minimum amplitude that sets the gain of corresponding gain stage 302(i) to a minimum value.

[00102] In a third configuration, switch 1204(i) connects ramp signals 1108 and 1110 to differential driver 1210(i) such that gain control signal 120(i) has an amplitude that follows a rising or increasing ramp function. For example, gain control signal 120(i) has an amplitude that increases over a time interval continuously and smoothly from the minimum amplitude to the maximum amplitude. As a result, the gain of corresponding gain stage 302(i) increases over the time interval continuously and smoothly from the minimum gain to the maximum gain for that gain stage.

[00103] In a fourth configuration, switch 1204(i) connects ramp signals 1108 and 1110 to differential driver 1210(i), in a manner that is inverted with respect to the third configuration, such that gain control signal 120(i) has an amplitude that follows a falling or decreasing ramp function. For example, gain control signal 120(i) has an amplitude that decreases over a time interval continuously and smoothly from the maximum amplitude to the minimum amplitude. As a result, the gain of corresponding gain stage 302(i) decreases over the time interval continuously and smoothly from the maximum gain to the minimum gain for that gain stage.



**[00104]** When the aggregate gain of amplifier array **204** is to be maintained at a present value, first gain stages among gain stages **302** of VGA **204** are set to their respective maximum gains, while second gain stages among gain stages **302** of VGA **204** are set to zero gain. This type of arrangement was described above in connection with Steps 1, 3 and 5 of **FIG. 10A**. To effect such an arrangement:

(i) first switches (among switches **1204**) corresponding to the first gain stages of VGA **204** are set to their first configurations, so as to produce corresponding gain control signals at their maximum fixed amplitudes; and

(ii) second switches (among switches **1204**) corresponding to the second gain stages of VGA **204** are set to their second configurations, so as to produce corresponding gain control signals at their minimum fixed amplitudes.

**[00105]** When an aggregate gain change is required, the gain of one of the first gain stages is decreased to zero and the gain of one of the second amplifiers is increased to its maximum gain. This arrangement was described above in connection with Steps 2 and 4 of **FIG. 10A**. To achieve this, the switch corresponding to the one of the first gain stages (to be turned OFF) is placed into its third configuration and the switch corresponding to the one of the second amplifiers to be turned ON is placed in its fourth configuration. Then, the amplitudes of the gain control signals corresponding to these switches will ramp-up (e.g., increase) and ramp-down (e.g., decrease) as a function of ramp signals **1108** and **1110**. In turn, the gains of the corresponding gain stages will ramp-up and ramp-down.

**[00106]** **FIG. 13** is a block diagram of an example arrangement of power detector **216**. Also depicted in **FIG. 13** are exemplary signal waveforms corresponding to various portions of the power detector circuit. Power detector **216** includes an envelope detector **1302** followed by a low pass filter. The low pass filter includes a resistor (R) and a capacitor (C). Power detector **216** produces power level signal **230** at a voltage level (PDET) that is proportional to the amplitude or power level of amplified signal **118(2)**.

[00107] **FIG. 14** is a circuit diagram of an example arrangement of comparator **222**. Comparator **222** includes an upper threshold comparator **1402** for comparing power level signal **230** to upper threshold **224a**, to produce an upper threshold result **232a**. Upper threshold result **232a** indicates whether power level signal **230** is above or below upper threshold **224a**. Comparator **222** includes a target threshold comparator **1404** for comparing power level signal **230** to target threshold **228a**, to produce a target threshold result **232b**. Result **232b** indicates whether power level signal **230** is above or below target threshold **228a**. Comparator **222** also includes a lower threshold comparator **1406** for comparing power signal **230** to lower threshold **226a**, to produce a lower threshold comparison result **232c**. Result **232c** indicates whether power level signal **230** is above or below lower threshold **226a**. Comparison result signal **232** comprises the set of comparison results **232a-232c**.

[00108] **FIG. 15** is a circuit diagram of an example arrangement of a ramp generator **1500** of signal generator **242**. Also depicted in **FIG. 15** are exemplary signal waveforms corresponding to various nodes in the circuit **1500** (for example, waveforms corresponding to signals **1108** (VRAMP\_P), **1110** (VRAM\_N), and VRAMP). Ramp generator **1500** includes a first stage **1502**. First stage **1502** include a ramp generator switch **1504** coupled to a positive input of an operational transconductance amplifier (OTA) through a resistive voltage divider including resistors **R10** and **R11**. A current source **I1** is connected between the positive input of OTA **1508** and a power supply rail at voltage **VDD**. OTA **1508** is configured as a voltage follower amplifier having a current output. First stage **1502** also includes capacitor **244** ( $C_{EXT}$ ) connected between an output terminal or node **1514** of OTA **1508** and ground. Switch **1504** is selectively opened or closed (i.e., either disconnected from ground or connected to ground) responsive to a ramp trigger signal, which is one of control signals **1104** from controller **233**.

[00109] Assume initially that switch **1504** is open. When controller **233** closes switch **1504**, a voltage **VSW** at the positive input of OTA **1508** becomes 0.5 volts. Then, when controller **233** opens switch **1104**, the voltage **VSW** instantaneously jumps up to 1.5 volts. However, the output of OTA **1508**, that

is, the voltage VRAMP at node **1514** rises relatively slowly from 0.5 volts because the current produced by OTA **1508** charges capacitor **244**. OTA **1508** has a differential voltage input and a current output (or even a differential voltage output). OTA **1508** is advantageous in this application because it produces a slow, smooth and continuous, linear voltage change at its output due to the large capacitance of capacitor **244**. When controller **233** opens switch **1504**, the voltage VSW instantaneously drops to 0.5 volts. However, the voltage VRAMP at node **1514** drops slowly from 1.5 volts down to 0.5 volts because of a discharge effect caused by capacitor **244**. Any circuit that produces such a step voltage at the OTA input can be used in the present invention.

[00110] Ramp generator **1500** includes a second stage **1520** coupled to output node **1514**. Second stage **1520** includes an optional first voltage follower amplifier **1522** for generating signal **1108** (VRAMP\_P) and a second amplifier **1524** for generating signal **1110** (VRAMP\_N). Thus, complimentary ramp signals **1108** and **1110** can be made to ramp-up or ramp-down on command by selectively opening and closing switch **1504**.

[00111] The capacitance of capacitor **244** controls the slew time of ramp signal VRAMP (and correspondingly, the slew rates of ramp signals **1108** (VRAMP\_P) and **1110** (VRAMP\_N)). The example slew time depicted in FIG. 15 is one milliseconds (ms). However a range of slew times, for example, between one ms and ten ms, may be used in the present invention. The capacitance of capacitor **244** is relatively large, for example, in the range of ten (10) nanoFarads. Thus, it is advantageous to have capacitor **244** off-chip, so as to correspondingly reduce the size of IC chip **202**.

[00112] FIG. 16 is a circuit diagram of an example arrangement of a reference signal generator **1600** of signal generator **242**. Reference signal generator **1600** includes the following components connected in series and between a power supply rail at voltage VDD and ground: a current source **1602** and resistors **1604-1610**. Reference signal **1112** (VREF\_HI) is tapped-off between current source **1602** and resistor **1604**. Signal **1114** (VREF\_LO) is tapped-off between resistors **1608** and **1610**.

[00113] Reference signal generator 1600 also includes a ramp window comparator 1618 including first and second comparators 1622 and 1624. First and second comparators 1622 and 1624 compare the voltage VRAMP, generated at the output of OTA 1508 (discussed in connection with FIG. 15), to respective tapped voltages VREF2 and VREF1. Voltages VREF2 and VREF1 are tapped-off between resistors 1604 and 1606, and between 1606 and 1608, respectively. Comparators 1622 and 1624 generate ramp state signal 1106 indicating whether VRAMP (and correspondingly, whether signals 1108 and 1110) has settled to a static value, that is, finished slewing, after switch 1504 has either opened or closed. After controller 233 commands ramp generator 1502 to generate ramp VRAMP, by toggling switch 1504 either open or closed, the controller monitors ramp state signal 1106 to determine when the ramp has finished slewing to its final high or low fixed voltage.

#### V. Process Monitor

[00114] FIG. 16A is a circuit/block diagram of an example arrangement of process monitor 108, mentioned above in connection with FIGs. 1 and 2. The component values and transistor characteristics of a typical IC chip vary from one chip to another. Although ratios between one component and another match well on-chip, absolute values can vary widely. Process monitor 108 measures the absolute value of unit sample resistors and transistors. If a particular resistor or transistor measures high by a certain percentage, then all other resistors and transistors of that type will also measure high by the same amount. This information can be used to adjust the gain of an amplifier on the chip (for example, any of amplifiers 204 and 206 on IC chip 202) to a desired value, or to determine the true, corrected gain of such an amplifier. At any given time during the operation of amplifier assembly 102, the gain value of VGA 204 can be read through CI 109. Also, process information about process variations corresponding to IC chip 202 can be collected from process monitor 108. Based on the gain value, and the process information, gain

correction factors can be derived, and then applied to any of amplifiers 204 and 206 to compensate for the process variations.

[00115] Process monitor 108 includes the following circuits: a bias circuit 1650, a sense circuit module 1651, a multiplexer 1652, an amplifier 1653, a latched-comparator 1655, and a digital-to-analog converter (DAC) 1658.

[00116] Bias circuit 1650 produces a set of controlled, predetermined bias currents 1660. Responsive to bias currents 1660 and a select signal 1661, sense circuit module 1651 produces various sensed signals 1663 indicative of process parameters of IC chip 202, and provides the sensed signals to multiplexer 1652. Responsive to a multiplexer select signal 1664, multiplexer 1652 provides a selected one of sensed signals 1663 to the group of circuits 1653, 1655, and 1658. A value of the selected sensed signal is determined using circuits 1653, 1655 and 1658.

[00117] Bias circuit 1650 produces bias currents 1660 based on either CTAT (constant-to-absolute temperature, which remains constant as temperature changes) or PTAT (proportional-to-absolute temperature, which increases linearly with absolute (Kelvin) temperature). In addition, each current of bias currents 1660 is based on a particular resistor type, such as an external (off-chip, and assumed to have a very low temperature coefficient), poly-high (high sheet-rho polysilicon, on-chip) or poly-low (low sheet-rho polysilicon, on-chip). "Poly" means polysilicon, and "sheet-rho" refers to resistivity per unit area of the IC chip. Each type of current is labeled accordingly: "CTAT Ext\_R," "PTAT poly\_high," or "CTAT poly-high." Other on-chip resistors, such as diffused resistors, can be used.

[00118] FIG. 16B is a circuit diagram of an example arrangement of sense circuit module 1651. Also depicted in FIG. 16B is a portion of bias circuit 1650. Module 1651 includes a plurality of process monitor or sense circuits 1670-1680 for monitoring/sensing process-dependent parameters of IC chip or substrate 202. Module 1651 also includes a temperature monitor 1682. Switches S1-S5, controlled by signal 1661, apply appropriate ones of bias currents 1660 to various diode-connected transistors and grounded resistors of sense circuits 1670-1682. In response, sense circuits 1670-1682 produce

sensed signals 1663 having values that provide information about process variations and temperature of IC chip 202. In the arrangement depicted in FIG. 16B, sensed signals 1663 are voltages. In an alternative arrangement, the sensed signals may be currents. Alternatively, a mix of voltages and currents may be generated.

[00119] Monitor or sense circuit 1670 monitors or senses an NMOS conductivity (k) of IC chip or substrate 202. Sense circuit 1670 produces a sensed signal nmos\_k indicative of the NMOS conductivity.

[00120] Sense circuit 1672 monitors a PMOS conductivity of IC chip 202. Sense circuit 1672 produces a signal pmos\_k indicative of the PMOS conductivity.

[00121] In sense circuits 1670 and 1672, transistors M1 and M2 are relatively small MOS transistors running at high current density, in a diode-connected set-up. This causes their VGS to be much larger than the transistor threshold voltage (VTH, indicated in labels “vt” and “Vt” in FIG. 16B). Thus, this configuration provides information about the transconductance parameter, k, of the transistors on the IC chip. Since VGS is large for these devices, a two-resistor voltage divider is used to reduce the sense voltage to within the same range of the other sense circuits.

[00122] Sense circuit 1674 monitors an NMOS transistor threshold (vt) of IC chip 202. Sense circuit 1674 produces a signal nmos\_vt indicative of the NMOS threshold.

[00123] Sense circuit 1676 monitors a PMOS transistor threshold of IC chip 202. Sense circuit 1674 produces a signal pmos\_vt indicative of the PMOS threshold.

[00124] In sense circuits 1674 and 1676, transistors M3 and M4 are also diode-connected, and are large devices running at low current density. This causes these device to have a VGS near their VTH.

[00125] Sense circuit 1678 monitors a resistivity per unit area, poly-low sheet-rho of IC chip 202. Sense circuit 1678 produces a signal pl\_rho indicative of the resistivity per unit area, poly-low sheet-rho of IC chip 202.

- [00126] Sense circuit **1680** monitors a resistivity per unit area, poly-high sheet-rho of IC chip **202**. Sense circuit **1680** produces a signal `ph_rho` indicative of the resistivity per unit area, poly-high sheet-rho of IC chip **202**.
- [00127] In sense circuits **1678** and **1680**, two resistors, **R5** and **R6** are **3.75K** ohm poly-low and poly-high resistors (respectively) that are biased at a fixed current (external **R**, **CTAT**). The voltage across these resistors is proportional to the sheet-rho of each resistor.
- [00128] Sense circuit **1682** monitors a temperature of IC chip **202**, and produces a signal `therm` indicative of this temperature. In sense circuit **1682**, resistor **R7** is used to determine chip temperature. This is done by connecting either poly-high/**CTAT** or poly-high/**PTAT** reference current to this resistor. Since the reference current is based on a poly-high resistor in both cases, the effects of process variation on the poly-high resistor is removed, leaving only **CTAT** vs. **PTAT** variations (i.e. temperature variations).
- [00129] Referring again to **FIG. 16A**, multiplexer **1652**, amplifier **1653**, comparator **1655** and DAC **1658** cooperate with **CI 109** to determine the values of the various sensed signals **1663**. Multiplexer **1652** selects any one of sensed signals **1663**, responsive to control signal **1664**. Amplifier **1653** scales the selected sensed signal, and presents the scaled, selected sensed signal to latching comparator **1655**. Amplifier **1653** has an output voltage range between 0.5 and 1.5 volts, approximately, which is the same as the output range of DAC **1658**. Comparator **1655** is in a latch mode when its clock input is a logic “1,” and in a track (or transparent) mode when its clock input is a logic “0.” At the same time, switches **S1-S5** apply bias current(s) to the sense circuit(s) that produce(s) the selected sensed signal(s).
- [00130] **IC 109** applies an input `vref` to DAC **1658**. Namely, an input of “000000” produces 0.5 volts at the DAC output, while “111111” produces 1.5 volts. DAC **1658** applies its output to a comparison input of comparator **1655**. Comparator **1655** compares the DAC output voltage to the selected scaled sensed signal from the corresponding sense circuit, and produces comparison result output `comp_out`. **CI 109** accesses or reads the value of `comp_out`. Comparator **1655** uses a successive-approximation-register (**SAR**) algorithm

to determine the value, e.g., voltage, of the sensed signal by comparing the sense signal against the DAC output voltage with 6-bit resolution. The SAR operation is controlled through CI 109 (e.g., by external controller 112), which sets the DAC input bits (and hence its output voltage) and clocks the comparator. If the output of the comparator is a logic “1” after clocking, the sensed signal or voltage (at the scaling amplifier output) was larger than the DAC voltage (and vice-versa).

[00131] Multiplexer 1652, amplifier 1653, comparator 1655 and DAC 1658 cooperate with CI 109 to determine the values of the various sensed signals 1663. Any other circuit may be used to perform this function. In an alternative arrangement, sense module 1651 generates sensed signals 1663 as digital signals, for example, using an analog-to-digital converter (ADC) on the output of each sense circuit in module 1651, and presents the digital signals to CI 109. In this arrangement, circuits 1652, 1653, 1655 and 1658 may be omitted.

## VI. Method Flow Charts

[00132] FIG. 17 is a flowchart of an example method 1700 of controlling gain that may be performed in amplifier assembly 102. An initial step 1704 includes setting a gain of a VGA module, for example, amplifier module 104. For example, this step includes setting an initial gain of first stage amplifier 204, e.g., amplifier array 204, in accordance with gain control signals 120, and setting initial gains of second stage amplifiers 206 to programmed gain values. The gains may be set to any desired gain values. For the purposes of gain changes that may occur in subsequent steps of method 1700, amplifiers 206 can be considered to have relatively fixed gain set to initial values in step 1704, as compared to VGA 204, which has a relatively dynamic gain.

[00133] A next step 1710 includes amplifying a receive signal to produce an amplified signal. For example, this step includes amplifying receive signal 114 with amplifier array 204 and second stage amplifier 206(2) to produce amplified signal 118(2).



[00134] A next step 1715 includes detecting a power level of the amplified receive signal generated in step 1710. For example, power detector 216 detects the power level/amplitude of signal 118(2), to produce power level signal 230. Power level signal 230 is indicative of the power level of receive signal 114, and amplified signals 210 and 118.

[00135] A next step 1720 includes determining whether the power level of the amplified signal (as indicated by the detected amplified signal) is between an upper threshold (e.g., threshold 224a) and a lower threshold (e.g., threshold 226a) defining an AGC window. Step 1720 includes further steps 1722 and 1724. Step 1722 includes comparing the detected power level (“DPL”) to the upper threshold, and step 1724 includes comparing the detected power level to the lower threshold. If the detected power level of the amplified signal is between the upper and lower thresholds, that is, within the AGC window, then flow proceeds back to step 1710 through a delay or wait step 1724a. Step 1724a corresponds to a programmable time interval, and may be included in step 1724. Steps 1720 and 1724a may be performed under the control of controller module 220.

[00136] If the power level of the amplified signal is not between the upper and lower thresholds, that is, within the AGC window, then flow proceeds to a next step 1725. Step 1725 includes changing the gain of the VGA module so as to drive the power level of the amplified signal in a direction toward a target threshold (e.g., threshold 228a) intermediate the upper and lower thresholds. Step 1725 includes changing the gain until the power level of the amplified signal crosses the target threshold. The gain change is smooth and continuous, in accordance with a ramp function.

[00137] Step 1725 includes further steps 1730 and 1735. Step 1730 includes decreasing the gain when comparison step 1722 indicates the power level of the amplified signal is above the upper threshold. Step 1735 includes increasing the gain when comparison step 1724 indicates the amplified signal power level signal is below the lower threshold. Step 1725 may be performed under the control of controller module 220. For example, controller 220

generates control signals **120** so as to change the gain of amplifier array **204**, and thus, the gain of amplifier module **104**.

[00138] After the gain change of step **1725**, flow proceeds back to step **1710** through a delay or wait step **1737** (similar to wait step **1724a**), and the process described above repeats. Step **1737** corresponds to a programmable time interval, and may be included in both of steps **1730** and **1735**.

[00139] In an alternative arrangement of method **1700**, the gains of both amplifiers **204** and **206** may be changed in step **1725**.

[00140] The example gain change scenarios discussed above in connection with **FIGs. 10A** and **10B** may be achieved in accordance with method **1700**. For example, at sample time **1052** in **FIG. 10B** (corresponding to step **1722** in method **1700**), controller module **220** determines or becomes aware that the gain of VGA **204** needs to be reduced. In response, controller module **220** reduces the gain of VGA **204** between times **1052** and **1054** (corresponding to step **1730** of method **1700**), that is, until the power level signal crosses target threshold **228a**. Controller module **220** reduced the gain of VGA **204** in accordance with the gain change scenario of **FIG. 10A**. Then, as depicted in **FIG. 10B**, controller module **220** waits until a next sample time (corresponding to wait step **1737** in method **1700**), before again polling comparison result signal **232** to test whether another gain change is required.

[00141] Frequent AGC induced gain changes can sometimes cause disruptive amplitude changes in an AGC controlled output signal. For example, the frequent AGC induced gain changes can sometimes disrupt the operation of circuits or processors, such as demodulators, that process the AGC controlled output signal. The present invention advantageously reduces the frequency of AGC induced gain changes compared to conventional AGC systems. In the present invention, this advantageous effect arises from a combination of (i) polling comparison result signal **232** at spaced time intervals (e.g., every  $t_{\text{sample}}$ ) to determine if a gain change is required, and (ii) maintaining power level signal **230** at or near target threshold **228a**, within an AGC window, and then only changing the gain when the power level signal is outside of the AGC window. Either one of these techniques taken alone can reduce the frequency

of gain changes, but together these techniques even further reduce the frequency of gain changes.

[00142] **FIG. 18** is a flow chart expanding on initial gain setting step 1704, as performed in amplifier assembly 102. Step 1704 includes a further step 1802, wherein controller module 220 generates gain control signals 120 such that (i) first gain stages among gain stages 302 in VGA 204 are set to their respective maximum gains, and (ii) second gain stages among gain stages 302 in VGA 204 are set to zero gain. The control signals 120 corresponding to the first gain stages of VGA 204 have fixed maximum amplitudes, and the control signals corresponding to the second gain stages of VGA 204 have fixed minimum amplitudes. With reference again to FIG.2, in step 1802, CI 109 commands controller module 220 to cause the gain of VGA 204 to be set to the desired value.

[00143] **FIG. 19** is a flow chart expanding on gain change step 1725, as performed in amplifier assembly 102. It is assumed that before step 1725 is executed, VGA 204 is configured to have an aggregate gain as a result of first gain stages thereof being set to their respective maximum gains and second gain stages thereof being set to zero gain. A step 1905 includes sequentially decreasing the gains of one or more of the first gain stages to zero gain according to a ramp function. A step 1910 includes sequentially increasing the gains of one or more of the second gain stages, corresponding to the one or more of the first gain stages, to their respective maximum gains according to the ramp function. Steps 1905 and 1910 may be performed concurrently. Alternatively, steps 1905 and 1910 may be performed in series with each other and such that step 1905 precedes step 1910, or alternatively, in a reverse order. Method 1900 may be performed to either increase the aggregate gain (as would be the case in step 1730) or decrease the aggregate gain (as would be the case in step 1735).

[00144] **FIG. 20** is a flow chart of a low-level example method 2000 expanding on gain change step 1725 and focusing on operations performed by elements of controller module 220 during the gain change. As mentioned above, step 1725, and thus, method 2000, is invoked when step 1720 indicates an

aggregate gain change is required. For example, when controller 233 determines, in response to comparison result 232, that an aggregate gain change is required.

[00145] It is assumed that before method 2000 begins, step 1704 set the aggregate gain of VGA 204 to an initial value. In this condition, first gain stages among gain stages 302 of VGA 204 are set to their maximum gains and second gain stages among gain stages 302 of VGA 204 are set to their minimum gains, so as to set the aggregate gain of VGA 204 to the initial value. More specifically, in switch matrix 240:

- (i) first switches (among switches 1204) corresponding to the first gain stages are set to their first configurations, and thus, the corresponding first gain control signals are set to their maximum amplitudes; and

- (ii) second switches (among switches 1204) corresponding to the second gain stages are set to their second configurations, and thus, the corresponding second gain control signals are set to their minimum amplitudes.

[00146] In a first step 2005, controller 233 receives comparison result signal 232. In response, controller 233 indicates to switch matrix 240, via signals 238, the direction of the required gain change, and thus, which gain stage among the first gain stages is to be turned OFF, and which gain stage among the second gain stages is to be turned ON. Essentially, in response to comparison result 232, controller 233 selects which gain stages are to be turned OFF and ON to effect the gain change.

[00147] In a next step 2010, responsive to control signals 238, switch matrix 240 sets:

- (i) the switch corresponding to the gain stage to be turned OFF to either its third or fourth configuration, as appropriate; and

- (ii) the switch corresponding to the gain stage to be turned ON to either its fourth or third configuration, as appropriate.

[00148] Essentially, the gain control signals corresponding to these two switches are connected to the output of the ramp generator, and are thus are ready to be driven by a ramp signal.

[00149] In a next step **2015**, controller **233** triggers ramp generator **1502** to generate the ramp signals **1108** and **1110** according to the ramp function, e.g., by toggling switch **1504**. In response to ramp signals **1108** and **1110**, the gain control signals corresponding to the switches coupled to ramp generator **1502** turn OFF and ON their corresponding gain stages.

[00150] In a next step **2020**, controller **233** monitors ramp state signal **1106** to determine when ramp signals **1108** and **1110** have settled to their final fixed values, that is, when the ramp has finished slewing. When this occurs, controller **233** sets:

(i) the switch corresponding to the gain stage just turned OFF to either its first or second configuration, as appropriate; and

(ii) the switch corresponding to the gain stage just turned ON to either its second or first configuration, as appropriate.

[00151] Essentially, the gain control signals corresponding to these two switches are now connected to the output of the reference signal generator, and are thus held at respective fixed amplitudes.

[00152] In a next step **2025**, controller **233** determines if a further gain change is required. That is, controller **233** determines if power level signal **230** has still not crossed target threshold **238a**. The time delay involved in performing this step contributes to the pause between successive incremental gain changes discussed above in connection with **FIGs. 10B** and **10A**.

[00153] If step **2025** indicates no further gain change is required, then method **2000** stops. On the other hand, if step **2025** indicates a further gain change is required, then flow proceeds back to step **2005**, and the gain change process repeats. In this manner, method **2000** changes gain one step at a time, that is, in each iteration through steps **2005-2025**, until the power level signal **230** is at or near target threshold **238a**.

## VII. Example System - CATV Set-top Box

[00154] **FIG. 21** is a flow chart of another method of controlling the gain of **VGA 204**, in amplifier assembly **102**. **VGA 204** includes gain stages **302**

connected in parallel with each other and that collectively establish an aggregate gain of the VGA. The VGA receives gain control signals 120, each for controlling a gain of a corresponding one of parallel gain stages 302.

[00155] In a first step 2105, VGA 204 amplifies receive signal 114 in accordance with the aggregate gain to produce an amplified output signal 210.

[00156] In a next step 2110, power detector 216 produces detected power 230 indicative of a power of amplified signal 210 produced by the VGA.

In a next step 2115, comparator module 218 produces comparison result signal 232 indicative of a relative relationship between the detected power signal and thresholds 224a-228a.

[00157] In a next step 2120, ramp generator 1502 generates ramp signals 1108 and 1110 on command.

[00158] In a next step 2125, reference signal generator 1600 generates reference signals 1112 and 1114 having fixed amplitudes.

[00159] In a next step 2130, controller module 220 generates gain control signals 120 responsive to comparison result signal 232, reference signals 1112 and 1114, and ramp signals 1108 and 1110 (when the ramp signals are generated). Controller module 220 generates gain control signals 120 such that amplified output signal 210 maintains a substantially constant amplitude as the power of receive signal 114 varies over time.

[00160] FIG. 22 is a block diagram of an example system 2200, such as a CATV set-top box, in which amplifier assembly 102 may be used. Amplifier assembly 102 provides amplified signals 118(1)-118(n) to corresponding individual tuners 2204(1)-2204(2). Each signal 118(i) includes a plurality of CATV channels, as mentioned above. Each tuner 2204(i) selects a subset only, for example, one, of the many frequency channels presented in corresponding signal 118(i). Each tuner 2204(i) produces a signal 2206(i) including the selected channel only.

[00161] Tuners 2204(1)-2204(n) provide signals 2206(1)-2206(n) to corresponding ones of demodulators 2210(1)-2210(n), as depicted in FIG. 22. Each demodulator 2210(i) demodulates the selected channel presented in its corresponding signal 2206(i). Amplifier assembly 102, tuners 2204 and

demodulators **2210** may be all controlled by a controller, such as controller **112** discussed in connection with **FIG. 2** (but not shown in **FIG. 22**).

[00162] Due to the AGC operation of amplifier assembly **102**, as described above, each tuner-demodulator pair (**2204(i)-2210(i)**) advantageously receives a corresponding signal **118(i)** having (i) the plurality of frequency channels present in signal **114**, and (ii) a substantially constant aggregate power level, under fluctuating amplitude conditions of input signal **114**. The smooth and continuous gain change operation of amplifier assembly **102** advantageously avoids abrupt, disruptive power level discontinuities in signals **118**, and thus in signals **2206**. As a result, the gain changes in amplifier assembly **102** are transparent to demodulators **2210**. For example, demodulators **2210** can maintain a successful “lock” on, or tracking of, signals **2206** during gain changes in amplifier assembly **102** that compensate for substantial fluctuations in the power of input signal **114**. Another advantage of the amplifier assembly is that AGC induced gain changes are less frequent than in conventional systems, for the reasons mentioned above in connection with **FIG. 17**.

[00163] Another advantage is that the AGC operation of amplifier assembly **102** is autonomous, that is, the AGC in amplifier assembly operates without the need of any feedback signal, such as a receive power indicator, from either tuners **2204** or demodulators **2210**. Another advantage is that the power levels of signals **118** may be controlled individually using only one component in the system, namely, amplifier assembly **102**. Thus, each signal **118(i)** delivers the required power to each tuner-demodulator pair, and this required power may differ substantially between the tuner-demodulator pairs.

## VIII. Conclusion

[00164] Further benefits of the invention include, at least, and by way of example and not by limitation, the following:

[00165] High bandwidth (i.e. good frequency performance).

[00166] Low distortion, especially for large composite channel signals found in cable TV. This is due to connecting the amplifier outputs to VDD via external

inductors or ferrites and due to using a resistors and attenuators in the front end of the amplifier assembly (e.g., in the VGA).

[00167] Only enough gain reduction is used at the first amplifier stage of the amplifier assembly to insure the largest input signal condition can be met. This allows use of fewer gain stages in the VGA. Gain reduction is achieved through turning OFF gain stages.

[00168] Low noise figure.

[00169] Good input match (even at different gain settings).

[00170] Minimized distortion as the gain is changed. This is accomplished by fully turning OFF or ON all unused gain stages.

[00171] Power consumption is lowered as sequential gain stages of the VGA are turned OFF.

[00172] Noise figure degradation vs. gain reduction is less than 1:1 for lower gain settings, since attenuation comes at the output after the first 18 dB (done by turning OFF gain stages). This is important when the input signal level is high.

[00173] Increased AGC control range: More than 30 dB at **860** MHz and more than 35 dB at lower frequencies.

[00174] At a minimum, application is to cable modems, set-top box receivers and analog TV tuners.

[00175] Gain in one arrangement is controlled by a combination of selecting amplifiers connected to a tapped resistor ladder and by turning ON and OFF amplifier forming part of gain stages.

[00176] IC chip has been designed to use low-cost digital CMOS process. However this is not a limitation as other semiconductor processes could be used including bipolar (including SiGe), BiCMOS or Gallium Arsenide (GaAs) MESFET.

[00177] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail can be made therein without departing from the spirit and scope of the invention.



**[00178]** The present invention has been described above with the aid of circuit modules, functional building blocks, and method steps illustrating the performance of specified functions and relationships thereof. The boundaries of these circuit modules, functional building blocks and method steps have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed. Any such alternate boundaries are thus within the scope and spirit of the claimed invention. One skilled in the art will recognize that these circuit modules, functional building blocks and modules can be implemented by discrete components including digital and/or analog circuits, application specific integrated circuits, processors executing appropriate software, hardware, firmware and the like or any combination thereof. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.